

**LISTING OF CLAIMS**

1. (Currently Amended) A system, comprising:  
  
a circuit receiving an enable signal, the circuit enabled for an operation when the enable signal is in a first state and disabled for that operation when the enable signal is in a second state;  
  
and  
  
a regulator circuit operable responsive to the enable signal to selectively provide a current ~~supplied by a system power source~~ to the circuit at a first current value when the enable signal is in the first state and at a second current value when the enable signal is in the second state.
2. (Original) The system according to claim 1, wherein the regulator circuit comprises a plurality of current sources.
3. (Currently Amended) The system according to claim 2, wherein at least one of the plurality of current sources is selectively activated by ~~an~~ the enable signal.
4. (Original) The system according to claim 3, wherein the plurality of current sources form mirror branches of a current mirror.

5. (Original) The system according to claim 4, wherein the at least one of the plurality of current sources comprises a first transistor and a second transistor connected in series to the first transistor, wherein a control terminal of the first transistor is coupled to a control terminal of a transistor in a reference leg of the current mirror and a control terminal of the second transistor is coupled to the enable signal.

6. (Currently Amended) The system according to claim 3, further comprising a delay component responsive to the enable signal and operable to delay the activation of the at least one of the plurality of current sources relative to the enable signal being in ~~an enabling~~ the first state.

7. (Currently Amended) The system according to claim 6, wherein the delay component is coupled ~~between~~ to delay application of the enable signal ~~and to~~ the regulator circuit but not the circuit.

8. (Original) The system according to claim 6, wherein the delay component delays one of a rising edge and a falling edge of the enable signal by an amount that is greater than a delay of the other of the rising edge and the falling edge of the enable signal.

9. (Original) The system according to claim 1, wherein the circuit includes a memory device.

10. (Currently Amended) The system according to claim 9, wherein the memory device and the regulator circuit both receive ~~an~~ the enable signal, the current value provided by the regulator circuit being based upon a value of the enable signal such that the memory device is enabled for normal operation and receives the first current value when the enable signal is in the first state and the memory device is disabled from normal operation and receives the second current value when the enable signal is in the second state.

11. (Currently Amended) A system, comprising:  
a circuit with an enable signal input and operable for selectively enabling an operation to be performed in the circuit if the enable signal is in a first state and selectively disabling the operation if the enable signal is in the second state; and

a regulator circuit coupled between a system power source and the circuit and having a control input for controlling the amount of supply current available to the circuit , the control input receiving the enable signal and the regulator operating to supply a relatively higher non-zero current level to the circuit when the enable input is in the first state and supply a relatively lower non-zero current level to the circuit when the enable input is in the second state ~~wherein the enable input of the circuit and the control input of the regulator circuit are coupled one to the other.~~

12. (Currently Amended) The system according to claim 11, wherein the regulator circuit comprises a plurality of current sources, at least one of the plurality of current sources is activated by ~~an~~ the enable signal coupled to the control input of the regulator circuit.

13. (Original) The system according to claim 12, wherein the plurality of current sources form mirror branches of a current mirror.

14. (Original) The system according to claim 12, wherein the at least one of the plurality of current sources is adapted for receiving the enable signal.

15. (Original) The system according to claim 12, further comprising a delay component operable to delay the deactivation of the at least one of the plurality of current sources relative to the circuit being disabled.

16. (Currently Amended) The system according to claim 15, wherein the delay component is coupled ~~between~~ to delay application of the enable signal ~~and~~ to the regulator circuit.

17. (Original) The system according to claim 15, wherein the delay component delays one edge of the enable signal relative to a second edge of the enable signal.

18. (Original) The system according to claim 12, wherein the at least one of the plurality of current sources comprise a first transistor and a second transistor connected in series to the first transistor, and a control terminal of the second transistor is coupled to the enable signal.

19. (Currently Amended) The system according to claim 11, wherein the circuit includes a memory device, and the enable signal input is a chip enable input of the memory device.

20. (Original) The system according to claim 19, wherein the memory device and the regulator circuit receive the same enable signal.

21. (Currently Amended) A method, comprising the steps of:  
receiving an enable signal that enables circuit operation when the enable signal is in a first state and disables circuit operation when the enable signal is in a second state; and  
supplying a current to a the circuit having a current level ~~that is based on a value of the enable signal~~ at a first value if the enable signal is in the first state and at a second value if the enable signal is in the second state.

22. (Original) The method according to claim 21, wherein the step of supplying the current further comprises the step of:

activating any one or more of a plurality of current sources in a regulator circuit so as to control the current supplied to the circuit, based on the value of the enable signal.

23. (Original) The method according to claim 22, wherein the step of supplying the current further comprises the step of delaying current source deactivation relative to the current source activation.

24. (Original) The method according to claim 21, further comprising the step of selectively enabling an operation in the circuit based on the value of the enable signal.

25. (Original) The method according to claim 24, further comprising the steps of delaying the step of supplying a current relative to the step of selectively enabling an operation.

26. (Canceled).

27. (Currently Amended) A method, comprising the steps of:  
coupling a system power source to a circuit;  
applying an enable signal to the circuit, the circuit being enabled for operation when the enable signal is in a first state and disable for operation when the enable signal is in a second state; and

selectively limiting the current supplied by the system power source to the circuit to any of at least two distinct non-zero current levels in response to the enable signal such that the system power source supplies a higher non-zero current level to the circuit if the enable signal is in the first state and supplies a lower non-zero current level to the circuit if the enable signal is in the second state.

28. (Original) The method according to claim 27, wherein the step of selectively limiting the current comprises the steps of:

coupling a regulator circuit having a plurality of current sources between the system power source and the circuit, operable to supply the current to the circuit; and

selectively activating one or more of the plurality of current sources so as to limit the current supplied to the circuit to any of the at least two distinct non-zero current levels.

29. (Currently Amended) The method according to claim 28, wherein the step of selectively activating further comprises the steps of:

selectively activating the one or more of the plurality of current sources so as to limit the current supplied to the circuit to ~~a first~~ the higher non-zero current level when ~~an~~ the enable signal ~~is a~~ has the first value state; and

selectively activating one or more of the plurality of current sources so as to limit the current supplied to the circuit to ~~a second~~ the lower non-zero current level when the enable signal ~~is a~~ has the second value state.

30. (Original) The method according to claim 28, further comprising the step of delaying the current source deactivation relative to the current source activation.

31. (Canceled).

32. (Currently Amended) The method according to claim 27 ~~31~~, wherein the enable signal selectively enables a memory access operation to occur.